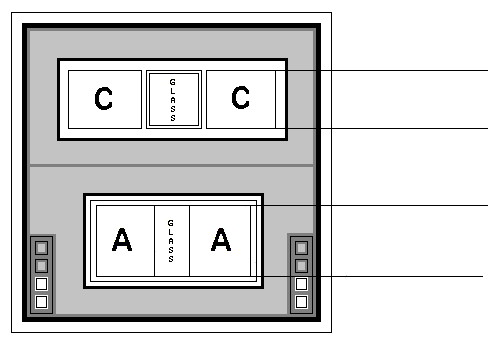
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**22 mils**

**22 mils**



**0.0045**

**0.004**

**Anode and Cathode on Top**

**Silicon Epitaxial Layer Construction for Low Series Resistance**

**Suried Zener Junction for High Reliablility**

**Silicon Nitride Passivation**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” min.**

**Backside Potential: Anode & Cathode on Top Surface**

**Mask Ref: ZHP**

**APPROVED BY: DK DIE SIZE .022” X .022” DATE: 8/31/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS .010” P/N: 1N4578A**

**DG 10.1.2**

#### Rev B, 7/19/02